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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/735,480	12/12/2003	Stephane Pinel	GTRC128	2478

6980 7590 11/19/2004

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EXAMINER	
LEE, GRANVILL D	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 11/19/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/735,480	PINEL ET AL.	
	Examiner	Art Unit	
	Granvill D Lee, Jr	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1- 14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 December 2003* is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-6 and 11-14 are rejected under 35 U.S.C. 102(e) as being anticipated by Kwong (US Pat. 6,732,428).

In view of these claims, Kwong teaches a method of embedding a circuit, comprising the steps of, providing a first layer of dielectric material (Fig. 2 #130), providing a circuit (#158) having a predetermined length, width, and depth (Col. 5 lines 30-35), forming a cavity in the first layer of dielectric material (#166) substantially corresponding to the predetermined length and width of the circuit, and depositing the circuit into the cavity.

In view of claim 2, Kwong teaches a method of providing the first layer of dielectric material comprising forming a layer of dielectric material at least as thick as the depth of the circuit (Fig. 2).

In view of claim 3, Kwong teaches a carrier (#128), where a first dielectric layer (#130) is placed thereon.

In view of claims 4, 5 and 13, glass carrier and photosensitive epoxy are structure limitations cited in a method claim and therefore are not given any significant patentable weight. Ex Parte Pfeiffer, 1962 C.D. 408 (1961).

In view of claim 6, Kwong teaches a method of embedding a circuit, comprising the steps of, providing a carrier (#128), providing a first layer (#130) of dielectric material, providing a circuit (#158) having a predetermined length, width, and depth, providing a second layer (#130) of dielectric material, forming a cavity (#166) in the second layer of dielectric material corresponding to the predetermined length and width of the circuit, depositing the circuit (Fig. 2) into the cavity; and providing a third layer (#132) of dielectric material.

In view of claim 11, Kwong further shows an embedded circuit module comprising, a first layer of dielectric material, a circuit having a predetermined length, width, and depth, a cavity in the first layer of dielectric material substantially corresponding to the predetermined length and width of the circuit; and wherein the circuit is embedded in the cavity (Col. 5 lines 20-40).

In view of claim 12, Kwong continues teaching wherein the first layer of dielectric material is at least as thick as the depth of the circuit (Fig. 1a or 2).

In continuing view of claim 14, Kwong shows a number of layers (incl. the 2nd) embedded with circuit devices (Fig. 2).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kwong (US Pat. 6,732,428) in view of In re Schering.

In view of claim 7, Kwong shows a method of conductive lines between dielectric layer in order to retrieve electrical signals from the circuit, but fails to show an actual hole or via in the design. Since it is inherent that some manner of retrieving electrical signals from buried or covered circuits is needed, a via or hole or similar structure would need to be formed with conduction member in order for the signal to be retrieved. Therefore, it would have been obvious to one having ordinary skill in the art at the time of the invention to consider the most cost effective design, and held that such designs involve only routine skill in the art. Schering Corp. v. Geneva Pharm Inc. 339 F.3d 1373, 1377, 67 USPQ2d 1664, 1668 (Fed Cir. 2003).

Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kwong (US Pat. 6,732,428) in view of In re Nerwin.

In view of claim 8, Kwong discloses a several dielectric layers, which make a multi-layered circuit board, but fails to show any single layer separated into a plurality of dielectric layers. Since it is notoriously well known to separate a layer into a plurality of layers, it would have been obvious to one having ordinary skill in the art at the time of invention to separate the layers if the design called for it. Since it has been held that constructing a formerly integral structure into a plurality of elements involves only routine skill in the art. Nerwin v. Erlichman, 168 USPQ 177, 179.

Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kwong (US Pat. 6,732,428) in view of Kelly et al. (US Pat. 6,143,117).

In regard to these claims, Kwong discloses a method of embedding a circuit, comprising the steps of, providing a first layer or sub-layer (clm. 9) of dielectric material, providing a circuit having a predetermined length, width, and depth, forming a cavity in the first layer of dielectric material substantially corresponding to the predetermined length and width of the circuit, followed by several (Fig. 2 #132,#130,#128) dielectric layers (Clm. 6) or sub-layers with cavities, but noticeably fails to include a carrier device portion with the design. Kelly et al. discloses a thin film structure where a carrier device is used in the device design (Title) and made of glass (Col. 4 lines 65-68).

Therefore, it would have been obvious to a person of ordinary skill in the

art at the time of the invention to modify the embedded circuit design of Kwong in favor of the temporary carrier design of Kelly et al. with the desire to conduct further testing on the device using the carrier, which can be discarded when testing or processing is complete. Kelly et al. saw that placing a faulty device on a permanent structure resulted in waste and increased cost (Col. 9 lines 37-47). Further, Kelly shows a number of dielectric layers which can be each designated as sub-layers of the overall multi-layered device (Col. 6 lines 55-68), followed by conductive material filling the vias.

Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kwong (US Pat. 6,732,428) in view of Volant et al. (US Pub. 2003/0148550)).

In view of this claim, Kwong discloses a method of embedding a circuit, comprising the steps of, providing a first layer of dielectric material, providing a circuit having a predetermined length, width, and depth, forming a cavity in the first layer of dielectric material substantially corresponding to the predetermined length and width of the circuit, yet fails to suggest sacrificial material used in the device design. Volant et al. discusses a method where sacrificial material is used in the cavities of a device.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to modify the device of Kwong with the back-filled cavity of Volant et al. in order to provide for further processing. Volant et al. determined that in order to continue with further processing area with vias

have to be filled with a sacrificial material upon which a beam or subsequent dielelctric layer can be further developed (Abstr. & Para. 37) or removed depending on design.

Contact Information

Any inquiry concerning this communication or earlier communications for the examiner should be directed to Granvill Lee whose telephone number is (571) 272-1897. The examiner can be normally reached on Monday thru Friday from 8:00 am to 4:30 pm.

If attempts to reach the examiner by telephone are not successful, the examiner's supervisor, Matthew Smith can be reached on (571) 272-1907. The fax phone number for this group is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Examiner
Granvill Lee
Art Unit 2825

Gl
11/7/04

MATTHEW SMITH
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